What is claimed is:

1. A fabrication method for a damascene bit line contact plug, comprising the steps of:

providing a semiconductor substrate having a first gate conductive structure, a second gate conductive structure and a source/drain region, in which the source drain region is formed in the substrate between the first gate conductive structure and the second gate conductive structure;

forming a first conductive layer in a space between the first gate conductive structure and the second gate conductive structure, in which the first conductive layer is electrically connected to the source/drain region;

forming an inter-layer dielectric with a planarized surface overlying the substrate to cover the first conductive layer, the first gate conductive structure, and the second gate conductive structure;

forming a bit line contact hole in the inter-layer dielectric to expose the top of the first conductive layer; and

forming a second conductive layer in the bit line contact hole, in which the combination of the second conductive layer and the first conductive layer serves as a damascene bit line contact plug.

2. The fabrication method for a damascene bit line contact plug as claimed in claim 1, wherein the formation of the first conductive layer comprises the steps of:

forming a first liner to covering the first gate conductive structure, the second gate conductive structure and the substrate;

providing a first photoresist layer having an opening corresponding to the bit line contact hole;

removing the first liner exposed within the opening to expose the source/drain region located between the first gate conductive structure and the second gate conductive structure;

removing the first photoresist layer;

depositing the first conductive layer to fill the space between the first gate conductive structure and the second gate conductive structure;

performing a chemical mechanical polishing process on the first conductive layer, in which the top of the first conductive layer is higher or approximately equal to the first liner positioned on top of the first gate conductive structure and the second gate conductive structure;

providing a second photoresist layer having a pattern corresponding to the bit line contact hole; and

removing the first conductive layer not covered by the second photoresist layer, in which the first conductive layer remains in the space between the first gate conductive structure and the second

gate conductive structure and is electrically connected to the source/drain region.

3. The fabrication method for a damascene bit line contact plug as claimed in claim 2, wherein the formation of the first conductive layer further comprises the steps of:

removing the second photoresist layer; and

performing a wet etching process to remove polymer residue from the substrate.

4. The fabrication method for a damascene bit line contact plug as claimed in claim 2, wherein the first liner is SiN or SiON.

5. The fabrication method for a damascene bit line contact plug as claimed in claim 2, wherein the thickness of the first liner is 100~120Å.

6. The fabrication method for a damascene bit line contact plug as claimed in claim 1, wherein the formation of the bit line contact hole comprises the steps of:

forming a second liner on the substrate;

forming a first inter-layer dielectric layer on the substrate to cover the second liner;

performing a chemical mechanical polishing process on the first inter-layer dielectric, in which the top of the first inter-layer dielectric is leveled off with the top of the second liner;

forming a second inter-layer dielectric to cover the first inter-layer dielectric and the second liner;

providing a third photoresist layer having an opening corresponding to the bit line contact hole; and

removing the second inter-layer dielectric and the second liner exposed within the opening to expose the top of the first conductive layer.

7. The fabrication method for a damascene bit line contact plug as claimed in claim 6, wherein the first liner is removed before forming the second liner, thus the second liner covers the first conductive layer, the first gate conductive structure and the second gate conductive structure.

8. The fabrication method for a damascene bit line contact plug as claimed in claim 6, wherein the second liner is formed on top of the first conductive layer, thus the combination of the first liner and the second liner covers the first conductive layer, the first gate conductive structure, and the second gate conductive structure.

9. The fabrication method for a damascene bit line contact plug as claimed in claim 6, wherein the second liner is SiN or SiON.

10. The fabrication method for a damascene bit line contact plug as claimed in claim 6, wherein the thickness of the second liner is 100~120Å.

11. The fabrication method for a damascene bit line contact plug as claimed in claim 6, wherein the first inter-layer dielectric is a BPSG layer.

12. The fabrication method for a damascene bit line contact plug as claimed in claim 6, wherein the thickness of the first inter-layer dielectric is 3500~3000Å.

13. The fabrication method for a damascene bit line contact plug as claimed in claim 6, wherein the second inter-layer dielectric is a TEOS oxide layer.

14. The fabrication method for a damascene bit line contact plug as claimed in claim 6, wherein the thickness of the second inter-layer dielectric is 3000~2500Å.

15. The fabrication method for a damascene bit line contact plug as claimed in claim 1, wherein the second conductive layer is tungsten, polysilicon or other conductive material.

16. A fabrication method for a damascene bit line contact plug, comprising the steps of:

providing a semiconductor substrate having a first gate conductive structure, a second gate conductive structure, a third gate conductive structure and a fourth gate conductive structure, in which the second gate conductive structure and the third gate conductive structure are formed within an active area;

forming a first conductive layer to fill the space between the second gate conductive structure and the third gate conductive structure;

forming a liner on the substrate to cover the first gate conductive structure, the second gate

conductive structure, the third gate conductive structure and the fourth gate conductive structure;

forming a first inter-layer dielectric to fill the space between the first gate conductive structure and the fourth gate conductive structure, and fill the space between the second gate conductive structure and the third gate conductive structure;

forming a second inter-layer dielectric on the first inter-layer dielectric;

forming a bit line contact hole, a gate contact hole and a source contact hole, in which the bit line contact hole exposes the top of the first conductive layer, the gate contact hole exposes the top of the first gate conductive structure, and the source contact hole exposes the substrate laterally adjacent to the fourth gate conductive structure; and

forming a second conductive layer to fill the bit line contact hole, the gate contact hole and the source contact hole, in which the second conductive layer formed in the bit line contact hole is electrically connected to the first conductive layer to serve as a damascene bit line contact plug.

17. The fabrication method for a damascene bit line contact plug as claimed in claim 16, wherein the semiconductor substrate further comprises a first shallow

trench isolation region and a second shallow trench isolation region to define the active area, in which the first shallow trench isolation region is formed between the first gate conductive structure and the second gate conductive structure, and the second shallow trench isolation region is formed between the third gate conductive structure and the fourth gate conductive structure.

18. The fabrication method for a damascene bit line contact plug as claimed in claim 16, wherein the semiconductor substrate further comprises:

a first source/drain region formed in the substrate between the second gate conductive structure and the third gate conductive structure; and

a second source/drain region formed in the substrate outside the active area and laterally adjacent to the fourth gate conductive structure;

wherein, the first conductive layer is electrically connected to the first source/drain region; and

wherein, the source contact hole exposes the second source/drain region.

19. The fabrication method for a damascene bit line contact plug as claimed in claim 16, wherein the formation of the bit line contact hole comprises the steps of:

forming a first liner on the substrate to cover the first gate conductive structure, the second gate conductive structure, the third gate conductive structure and the fourth gate conductive structure;

providing a first photoresist layer having an opening corresponding to the bit line contact hole;

removing the first liner exposed within the opening to expose the substrate between the second gate conductive structure and the third gate conductive structure;

removing the first photoresist layer;

depositing the first conductive layer to fill the space between the second gate conductive structure and the third gate conductive structure;

performing a chemical mechanical polishing process on the first conductive layer, in which the top of the first conductive layer is higher or approximately equal to the first liner positioned on top of the second gate conductive structure and the third gate conductive structure;

providing a second photoresist layer having a pattern corresponding to the bit line contact hole; and

removing the first conductive layer not covered by the second photoresist layer, in which the first conductive layer remains in the space between the second gate conductive structure and the third gate conductive structure.

20. The fabrication method for a damascene bit line contact plug as claimed in claim 19, wherein the formation of the first conductive layer further comprises the steps of:

removing the second photoresist layer; and

performing a wet etching process to remove polymer residue from the substrate.

21. The fabrication method for a damascene bit line contact plug as claimed in claim 19, wherein the first liner is SiN or SiON.

22. The fabrication method for a damascene bit line contact plug as claimed in claim 19, wherein the thickness of the first liner is 100~120Å.

23. The fabrication method for a damascene bit line contact plug as claimed in claim 16, wherein the formation of the bit line contact hole, the gate contact hole and the source contact hole comprises the steps of:

forming a second liner on the substrate;

forming a first inter-layer dielectric layer on the substrate to cover the second liner;

performing a chemical mechanical polishing process on the first inter-layer dielectric, in which the top of the first inter-layer dielectric is leveled off with the top of the second liner;

forming a second inter-layer dielectric to cover the first inter-layer dielectric and the second liner;

providing a third photoresist layer having a first opening corresponding to the bit line contact hole, a second opening corresponding to the gate contact hole, and a third opening corresponding to the source contact hole; and

removing the second inter-layer dielectric, the first inter-layer dielectric and the second liner exposed within the first opening, the second opening, and the third opening, thus exposing the top of the first conductive layer, the top of the first gate conductive structure and the substrate laterally adjacent to the fourth gate conductive structure.

24. The fabrication method for a damascene bit line contact plug as claimed in claim 23, wherein the first liner is removed before forming the second liner, thus the second liner covers the first conductive layer, the first gate conductive structure, the second gate conductive structure, the third gate conductive structure and the fourth gate conductive structure.

25. The fabrication method for a damascene bit line contact plug as claimed in claim 23, wherein the second liner is formed on top of the first conductive layer, thus the combination of the first liner and the second liner covers the first conductive layer, the first gate conductive structure, the second gate conductive structure, the third gate conductive structure and the fourth gate conductive structure.

26. The fabrication method for a damascene bit line contact plug as claimed in claim 23, wherein the second liner is SiN or SiON.

27. The fabrication method for a damascene bit line contact plug as claimed in claim 23, wherein the thickness of the second liner is 100~120Å.

28. The fabrication method for a damascene bit line contact plug as claimed in claim 23, wherein the first inter-layer dielectric is a BPSG layer.

29. The fabrication method for a damascene bit line contact plug as claimed in claim 23, wherein the thickness of the first inter-layer dielectric is 3500~3000Å.

30. The fabrication method for a damascene bit line contact plug as claimed in claim 23, wherein the second inter-layer dielectric is a TEOS oxide layer.

31. The fabrication method for a damascene bit line contact plug as claimed in claim 23, wherein the thickness of the second inter-layer dielectric is 3000~2500Å.

32. The fabrication method for a damascene bit line contact plug as claimed in claim 16, wherein the second conductive layer is tungsten, polysilicon or other conductive material.